



Implementation of a Wide Band and Low Noise Signal Generator Based on Phase Locked Loop

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ABSTRACT

A signal generator, an essential electronic test instrument with versatile applications, finds its utility in various fields such as cellular communications, radar systems, microstrip antennas, and electronics labs. This research focuses on the simulation and design of a low-phase noise signal generator operating in frequency range of 35 MHz to 3 GHz. To accomplish this, an Atmega 328P microcontroller on an Arduino board was employed to control the synthesizer based on the Phase-Locked-Loop (PLL) concept. The signal generator's performance was assessed, with particular emphasis on predicting and analyzing the phase noise generated by the PLL components. To ensure a robust system, a third-order loop filter was devised to effectively suppress spurs. Through simulation using the ADIsimPLL simulation tool, optimal values for loop bandwidth (10 kHz) and phase margin (45°) were obtained. The chosen Phase-Locked-Loop chip for this implementation was the ADF4351, manufactured by Analog Devices. By conducting transient analysis, the time required for the PLL system to transition from the minimum to the maximum output frequency was determined. Furthermore, the characteristics of the generator's signal were investigated in the frequency range of 35-100 MHz using a cathode ray oscilloscope, and for 101-3000 MHz using a spectrum analyzer. The phase noise levels were calculated at different frequencies (35 MHz, 387 MHz, 1 GHz, 2 GHz, and 2.9 GHz) and analyzed at varying offsets (1 kHz, 10 kHz, 100 kHz, and 1 MHz). Comparatively, the experimental results indicated a higher level of phase noise than what was obtained through simulation. Notably, as the output frequency increased, there was a corresponding increase in

the amount of phase noise. The maximum spur observed occurred at the third harmonic, measuring -18.6 dBc, while the minimum spur appeared at the fourth harmonic, measuring -44.5 dBc.

Keywords: Frequency synthesizer, Lock time, ADF4351, Loop filter, Phase-Locked-Loop, Voltage-controlled oscillator.

INTRODUCTION

A signal generator is an electronics test instrument that has a wide range of applications (Qi *et al.*, 2015). Some of these applications include testing systems in cellular communications, radar, microstrip antennas and testing components in electronics lab (Yuan and Chen, 2014). For a signal generator to be used in these applications, it should generate high frequencies, have a low level of phase noise, and also have a fast locking time. A frequency synthesizer can be defined as an electrical circuit that can generate a broad range of frequencies from a single frequency source (Fox, 2002). The common method of designing frequency synthesizers is by using phase-locked-loop (PLL) (Karthigeyan and Radha, 2020). A PLL is a control circuit with a feedback that is frequency or phase-sensitive and synchronizes a voltage-controlled oscillator (VCO) output signal with the signal of the reference oscillator (Vanhamel *et al.*, 2015). The phase/frequency detector (PFD) compares frequency or the phase of the reference oscillator to that of the VCO (Hati, and Bhattacharyya, 2018). The PFD can create two output signals, UP or DOWN, and this depends on deviation after synchronization (Li *et al.*, 2019). The charge pump

(CP) converts the signal from a phase or frequency state to a voltage state, which is used to vary the VCO. The VCO outputs a signal that depends on the voltage generated by the CP. When the output signal of PFD is high, the voltage output of CP increases, therefore, increasing the output frequency of VCO. Similarly, when the output of PFD is low, the output of the VCO decreases. The frequency generated by the VCO is then directed back to the PFD to recompute the variation in phase, hence creating a frequency control system that is closed-looped. This concept was used by Kameche and Feham (2013), in designing a synthesizer for exchanging data over short distances, operating in the industrial scientific and medical (ISM) band from 2400 MHz–2480 MHz with a 1 MHz frequency step. This design had a high phase noise of -82 dBc/Hz at 1 MHz offset frequency. Handique and Bezboruah (2015) designed and analysed a PLL based synthesizer to be applied in communication systems that are wireless. The design had low level of phase noise but the maximum output frequency was of 1.1 GHz.

The reference signal is always taken from a crystal oscillator since it produces stable frequencies. When the phase of the two signals has a difference of zero, the system is said to be locked. The main components of a PLL include a crystal oscillator, PFD, filter, CP, programmable frequency dividers and VCO (Curtin and O'brien, 1999) and (del Rocío Ricardez-Trejo *et al.*, 2017).

The divider can be manipulated to make the division ratio, N, either a whole number or a fraction, resulting in an integer-N PLL or a fractional-N PLL (Banerjee, 2017). Synthesizers based on PLL are commonly used in communication systems for wireless transmission because they have good resolution of the frequency and they lock quickly in time (Chenakin, 2017; Peng *et al.*, 2021). In this paper, a phase-locked-loop based signal generator which can generate frequencies in the range of 35 MHz - 3 GHz using a frequency synthesizer and a microcontroller to vary the output frequencies is designed. Fajar *et al.* (2019) designed a fractional based signal generator for detecting a high-resolution using a PLL and a microcontroller. This design had an output range of 0.5 GHz – 1.5 GHz and the phase noise was not analysed. The phase noise performance of the phase locked loop synthesizer has been improved using different methods. Hati and Bhattacharyya (2019) designed a constant loop bandwidth and phase noise cancellation in a wideband delta-sigma fractional-N PLL frequency synthesizer in the range of 2.158 GHz–5.133 GHz. They obtained low phase noise but their work did not look at low frequencies.

In this paper, a phase-locked-loop based signal generator which can generate frequencies in the range of 35 MHz - 3

GHz using a frequency synthesizer and a microcontroller to vary the output frequencies is designed.

METHODOLOGY

Phase-locked-loop frequency synthesizer design

The frequency synthesizer is designed using the ADF4351 PLL chip that enables building of either fractional-N or integer-N PLL (Fajar *et al.*, 2019). This chip is also integrated with a VCO whose output frequency ranges from 2200 MHz to 4400 MHz. The power supply of this chip is in the range of 3.0 V to 3.6 V.

The integrated chip registers are controlled via a Serial Peripheral Interface (SPI). The output of the frequency is given by equation 1 (Devices, 2008).

$$F_{OUT} = f_{PFD} \times \left(INT + \left(\frac{FRAC}{MOD} \right) \right) \quad (1)$$

where, FOUT is the output frequency, INTE is the value of the integer register (23 to 65,535), MOD is the value of the modulus register (2 to 4095), FRAC is the value of the fraction register (0 to MOD-1) and F P F D is the frequency of phase and frequency detector.

Loop filter design

In frequency synthesizers, a low pass filter that is designed using passive components is widely used. This is because passive filters have good phase noise performance and are simple to make compared to active filters (Paik *et al.*, 2016). The low pass filter suppresses the spurs produced by the PFD, which may cause unacceptable frequency modulation in the VCO (Shahruz, 2001). A 3rd order loop filter is designed in the simulation of the PLL as shown in Figure 1 in order to increase the attenuation of the spurs (Shurender *et al.*, 2013).

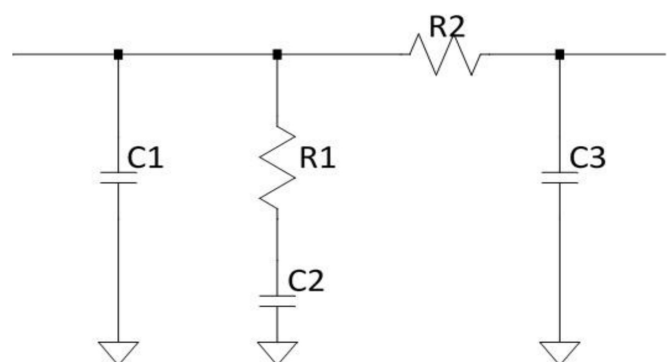


Figure 1: Topology of the Loop filter designed

The transfer function of a third order filter designed is given by equation 2 (Banerjee, 2017).

$$Z(s) = \frac{sC_2R_2 + 1}{s^2C_1C_2R_2 + sC_1 + sC_2} \quad (2)$$

One of the main parameters to pay attention to while designing PLL is the loop bandwidth. This parameter is affected by the components of the PLL, which include the filter, the VCO, the chip, and the reference oscillator.

Simulation of the PLL system

The simulations were done using ADIsimPLL design software. All key non-linear effects that affect PLL performance such as frequency transients and accurate models for phase noise were simulated. The loop bandwidth and phase values margin were changed in the simulation in order to get the optimum values for the filter.

High Frequency Signal Generator based on PLL

The signal generator was built by adding a section of a microcontroller that controls the PLL digitally through the SPI interface as shown in figure 2. The microcontroller used in this work was Atmega 328P on Arduino UNO board. An LCD keypad shield was also connected to the microcontroller to enable writing to and reading from the registers of the PLL chip. The selection of the output frequency was done by pressing the buttons on the keypad and it was displayed on the LCD.

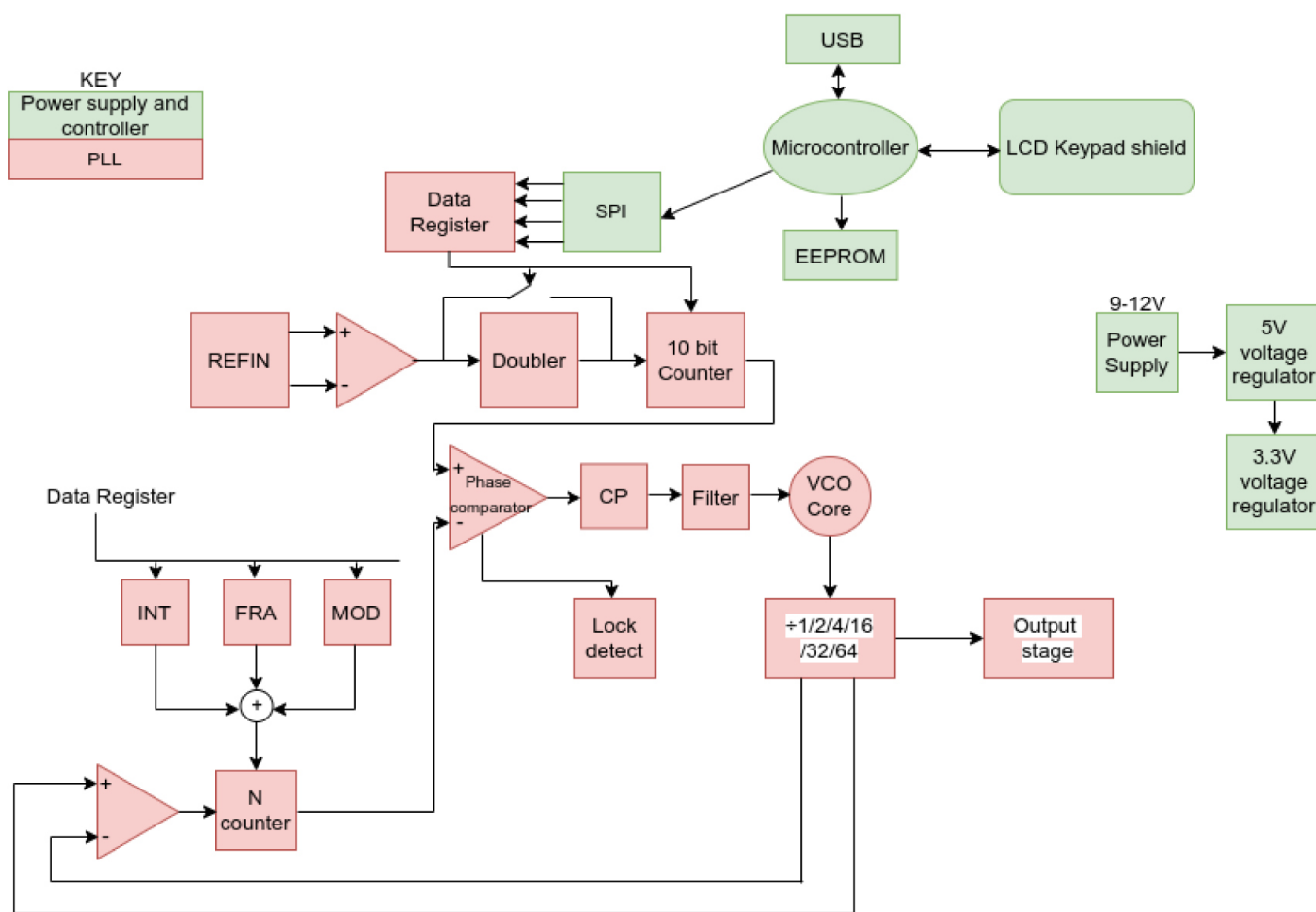


Figure 2: Architecture of high frequency signal generator based on PLL

Power supply design

Figure 3 shows the circuit diagram of the power module design. LM7805 is used in regulating the 15 V input to

a 5 V output which is used to power the microcontroller. LD1117av33 regulates the 5 V from LM7805 to 3.3 V which is used to power the ADF4351 chip.

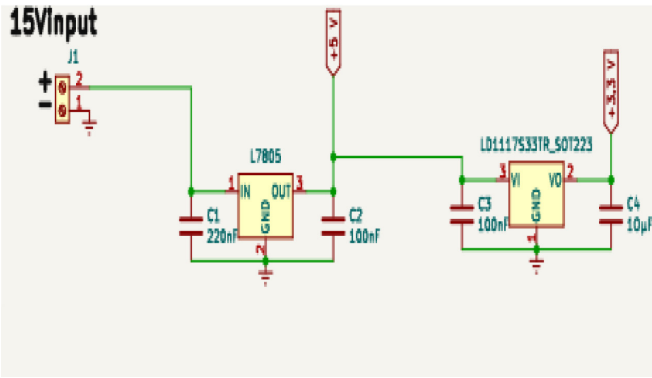


Figure 3: Circuit diagram of the power module

Synthesizer control design

Figure 4 shows the synthesizer and how it is controlled by Atmega 328P microcontroller. The 10 MHz reference frequency is fed to the ADF4351 synthesizer by capacitive coupling. The output of the charge pump is connected to a third order passive filter with a 10 kHz bandwidth and a phase margin of 45 .The output of the filter is then connected to the VTUNE input. The Serial Peripheral Interface (SPI) module of the Atmega 328P is used to set the registers of the synthesizer. Since the microcontroller works with 5 V, a voltage divider is formed using 560 Ω and 1 kΩ resistors to regulate the voltage to 3.3 V for CLK, DATA and load enable inputs of ADF4351.

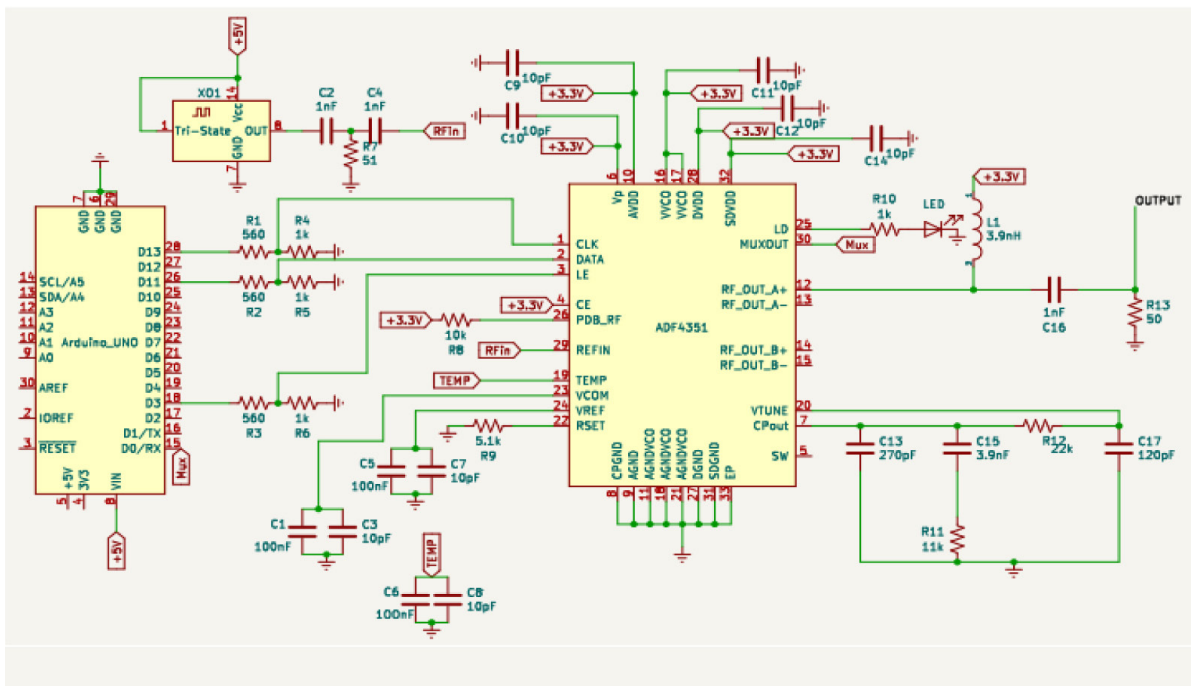


Figure 4: Circuit diagram of the power module

Keypad shield control

This shield consists of six momentary push buttons (select, up, right, down, left and reset) and a 2x16 LCD display, as shown in figure 4.17. The Arduino board is interfaced

with the LCD through pins 4, 5, 6, 7, 8, 9 and 10 as shown in Figure 5. All the buttons are connected to analog Pin 0, so ADC is used to read them. and the contrast of the LCD is varied using a potentiometer.

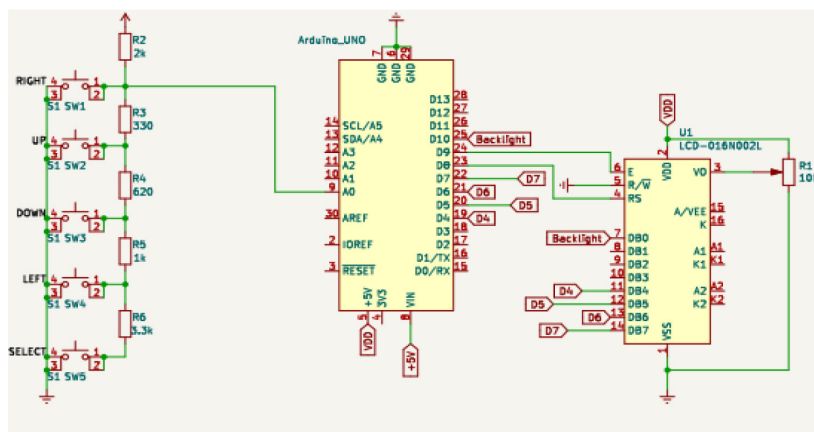


Figure 5: Circuit diagram of the keypad shield controlled by arduino

Calculation of phase noise and spurs

The phase noise was calculated using equation 3 (Banerjee, 2017).

$$PN = (L_c - L_o) - 10 \log_{10}(RBW) \quad (3)$$

where, L_c is the level of the carrier in dBm, L_o is the level at offset frequency in dBm and RBW is the resolution bandwidth of the filter in Hz. The level of spurs was calculated using equation 4.

$$Spurs = C_{power} - O_{power} \quad (4)$$

where C_{power} is the level of the carrier in dBm and O_{power} is the level of occurrence of spurs at a specific offset frequency.

RESULTS AND DISCUSSIONS

Loop Bandwidth optimization

The phase locked loop design was simulated for various loop bandwidths as shown in Table 1 and the phase noise and lock time of the bandwidths were analyzed.

Table 1: Simulation results for Loop Bandwidths at 100 kHz offset frequency

Loop Bandwidth(kHz)	Phase noise(dBc/Hz)	Lock time(us)
2.5	-129.53	2740
5.0	-129.02	1410
10.0	-125.96	753
20.0	-117.15	426
30.0	-110.59	317
40.0	-105.97	263
50.0	-102.63	230

The phase noise characteristics of these bandwidths were analysed as shown in Figure 6 from 100 Hz to 1 MHz offset frequency in order to determine the optimum loop bandwidth. It was observed that at 2.5 kHz and 5 kHz bandwidth, the phase noise was very high at lower frequencies and very low at higher frequencies. For the bandwidths beyond 10 kHz, the phase noise was very low at low offset frequencies but larger at high offset frequencies. The 10 kHz bandwidth was found to be optimum because it had the best phase noise characteristics compared to the rest. This is because it had low noise at low offsets compared to 2.5 kHz and 5 kHz bandwidths, and it had low phase noise at higher offset frequencies compared to 20 kHz and higher bandwidths, as shown in Figure 6. The phase noise of 10 kHz bandwidth at 1 MHz offset frequency was -150.80 dBc/Hz and was much lower compared to the phase noise of -82dBc/Hz at an offset frequency of 1MHz obtained by Kameche and Feham (2013).

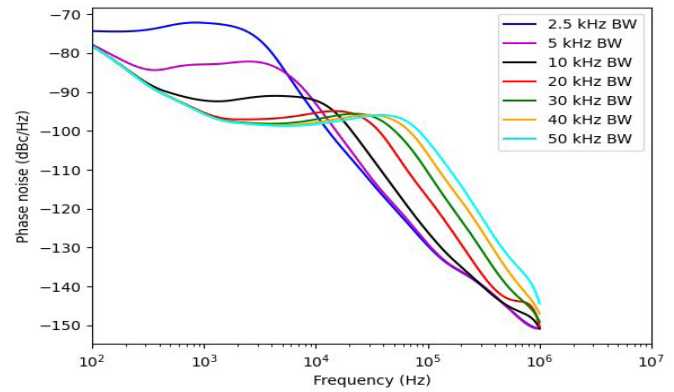


Figure 6: Phase noise simulation for different loop bandwidths

Phase Margin optimization

The phase margin values were varied from 35° to 60° . It was observed that the phase noise increased with an increase in phase margin as shown in Table 2. Therefore, the optimum value for phase margin was chosen as 45° because below this phase, the loop was unstable and the phase noise decreased compared to that of a 50° phase. The phase noise of the optimum phase margin was -125.96 dBc/Hz, and it was low compared to the phase noise obtained by Shrender *et al.* (2013) of -112.4 dBc/Hz at the same phase margin.

Table 2: Simulated results for various phase margin

Phase margin (degrees)	Phase noise (dBc/Hz)
35	-127.25
40	-126.69
45	-125.96
50	-124.95
55	-123.64
60	-121.66

The filter components obtained after simulation are as shown in Table 3.

Table 3: Optimized and standard values of filter components

Components	Optimized Value	Standard Value
Loop bandwidth	10 kHz	10 kHz
Phase margin	45°	47°
C_1	291 pF	270 pF
R_1	11.3 k Ω	11.0k Ω
C_2	3.96 nF	3.90 nF
R_2	23 k Ω	22 k Ω
C_3	133 pF	120 pF

Frequency domain analysis of the Phase-locked-loop

The plot of the simulated phase noise is illustrated in Figure 7. The noise of the reference dominated the characteristics at the earlier stages of the loop bandwidth, up to about 1

kHz. In the region between this frequency (1 kHz) and the loop bandwidth, the noise contributed by the chip and filter was effective as expected. A decrease in the slope is observed at the loop bandwidth of the system. This is because the phase noise contributed by the reference is quite low, while that of the chip, filter, and VCO starts to decrease. In the regions after the bandwidth, the noise of the VCO becomes the dominant factor, as expected, while the phase noise of other components starts to decrease continuously. At frequencies beyond 100 kHz, the total response follows the phase noise contributed by the VCO completely.

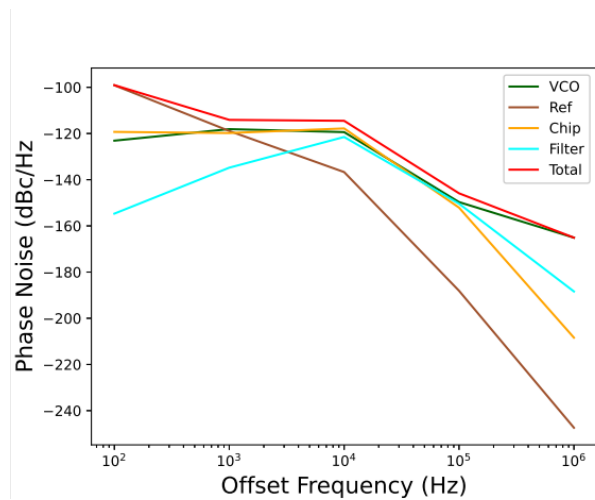


Figure 7: Contribution of the phase noise by the PLL system

The reference spurs which resulted from the non-linearity of the PFD in the signal path are shown in Figure 8. It can be seen from the plot that the first spurs occurring is a phase detector spur of -300 dBc because it occurs at an offset frequency the same as the phase detector frequency. The other spurs are modulated spurs and they are of -300 dBc.

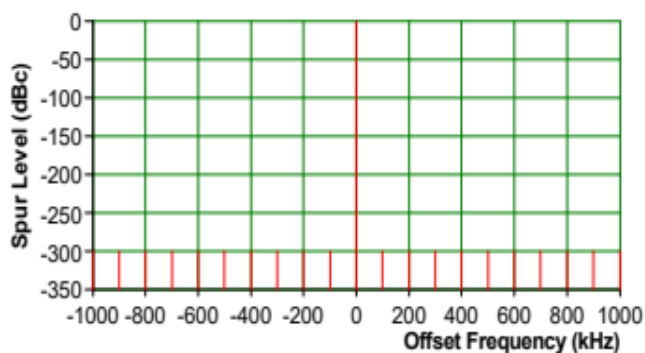


Figure 8: Reference spurs of the synthesizer at 387 MHz

Transient response of phase locked loop

As shown in Figure 9, transient response was simulated to show how the output frequency of the PLL changed. The PLL switched from 35 MHz-3 GHz and the lock time taken by the system to settle at 3 GHz was approximately

753 μ s. The locking time obtained was lower compared to 2.869 ms obtained by Hosseini-Tehrani and Masoumi (2017) and agrees with the one obtained by Shurender *et al.* (2013) of 119.5 μ s. The frequency first increased until it reached the peak frequency of about 3.18 GHz, and the absolute value of overshoot was 0.18 GHz. The rise time was almost 0 seconds while the peak time was approximately 9.27 μ s. After reaching the peak frequency, there was damping and repeated overshoot and undershoot (ringing) caused by the sudden change of frequency until the system reached a final frequency.

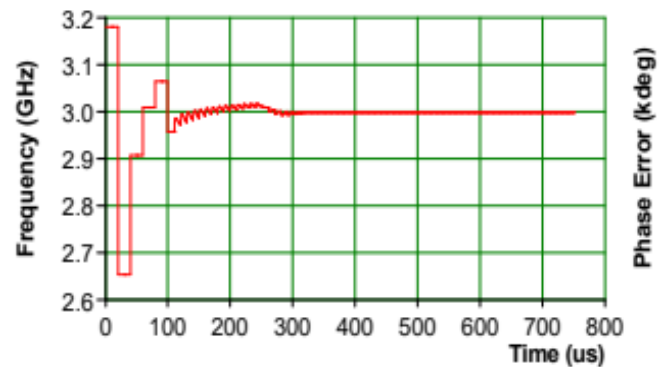


Figure 9: Transient frequency characteristics of simulated phase-locked-loop

Experimental Results

The output of the signal generator at 90 MHz was displayed on a cathode ray oscilloscope as shown in Figure 10.

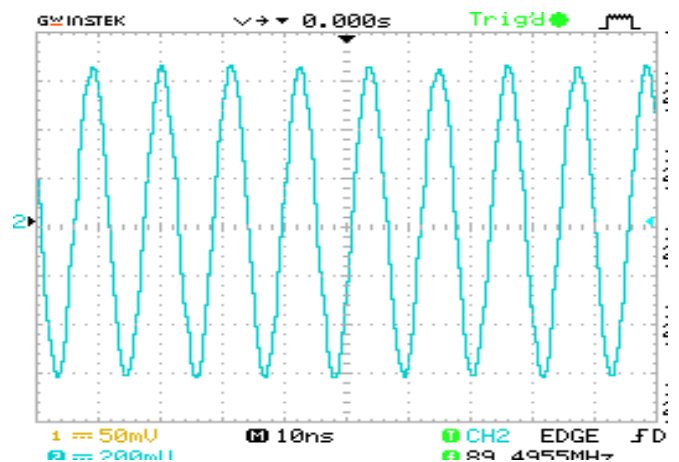


Figure 10: Output frequency of 90 MHz on a cathode ray oscilloscope

The output spectrum of the signal generator at 2.9 GHz is shown in Figure 11 with an output power of -58.4 dBm.

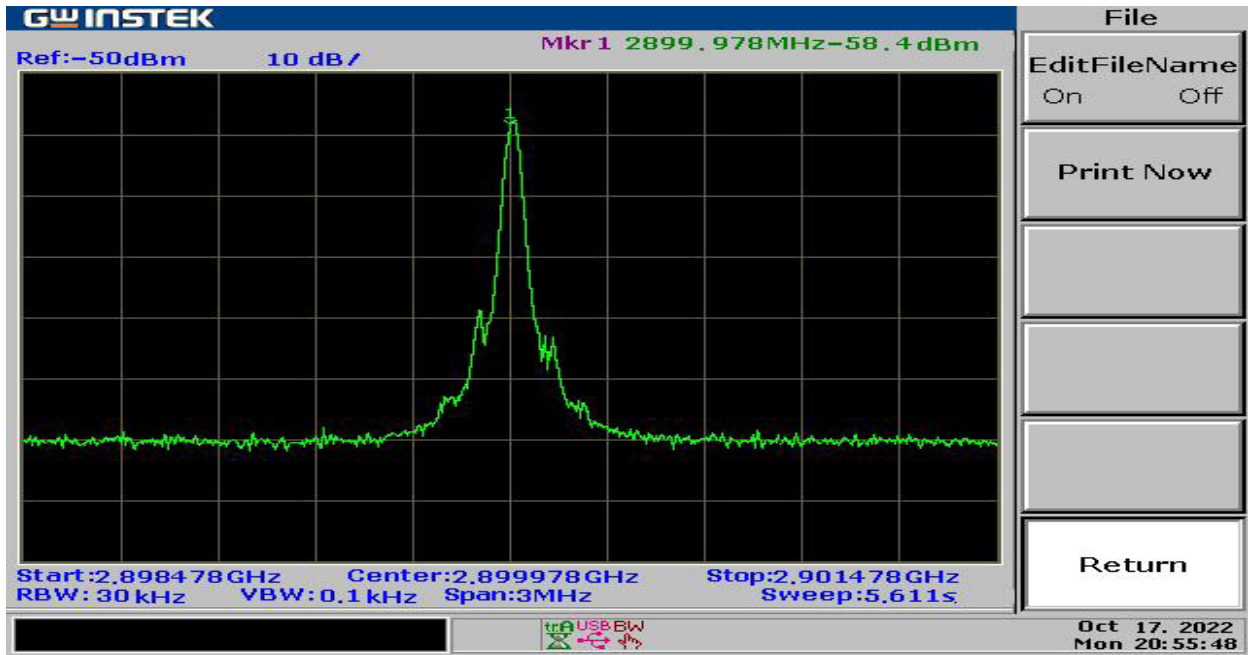


Figure 11: Output spectrum at 2900 MHz frequency on a spectrum Analyser

Experimental Phase Noise

The phase noise was calculated for 35.00 MHz, 387.00MHz, 1.00 GHz, 2.00 GHz and 2.90 GHz frequencies at 1 kHz, 10 kHz, 100 kHz and 1 MHz offset frequencies as shown in Table 4. The experimental phase noise agrees with the one obtained by Handique and

Bezboruah (2015) where they reported a phase noise of below 100 dBc/Hz at an offset frequency of 1 MHz in their study about design, fabrication and analysis of 1.1 GHz PLL synthesizer. Hosseini-Tehrani and Masoumi (2017) obtained a phase noise of below 100 dBc/Hz at an offset frequency of 100 kHz, agreeing with our results as in Table 4.

Table 4: Experimental Phase noise at 35.00 MHz, 387.00 MHz, 1 GHz, 2 GHz and 2.9 GHz

Offset frequency (kHz)	Experimental Phase Noise (dBc/Hz)				
	35 MHz	387 MHz	1 GHz	2 GHz	2.9 GHz
1	-94.2±1.2	-86.1±0.5	-76.5±0.5	-72.1±2.5	-71.2±1
10	-95.7±7	-90.3±1.5	-82.7±1	-77.9±1.5	-74.8±2
100	-106.4±1.5	-104.2±2	-102.6±1	-102.2±1	-100.7±2.6
1000	-115.7±3	-112.8±1	-112.1±0.5	-111.1±1	-110.7±1.5

The calculated phase noise, increasing with increase in the output frequency as shown in Figure 12, was also observed by Yang *et al.* (2012) in their design of Ultra-broadband, High Resolution Frequency Synthesizer. This is because the signal generator was implemented using the phase locked loop concept. For the phase locked loop to generate high frequencies and of wide range, the concept of frequency multiplication is carried out by using a counter to divide along the feedback loop. Therefore, as the frequency was multiplied to generate higher frequencies, the phase noise was raised by 20 multiplied by the logarithm of the value of the counter.

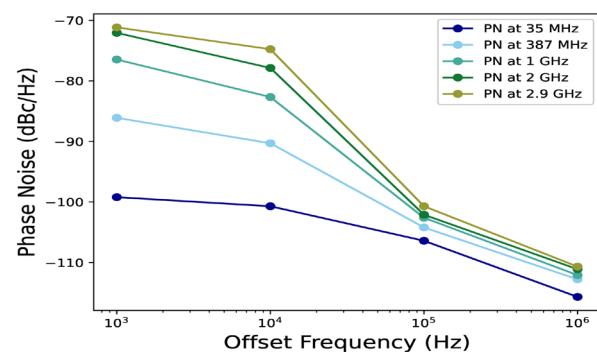


Figure 12: Phase Noise at 35 MHz, 387 MHz, 1 GHz, 2 GHz and 2.9 GHz output frequencies

The experimental phase noise was compared with the phase noise obtained after simulation for 387 MHz, 1 GHz, 2 GHz and 2.9 GHz as shown in Figure 13. From the graph, it can be seen that the experimental phase noise was higher compared to the simulated phase noise. This is because for the simulation, the phase noise contribution was from the phase locked loop components (Loop filter,

PLL chip, reference oscillator and the VCO) only while for the calculated, in addition to the phase noise from the PLL components, there were other sources of phase noise while carrying out the experiment. These sources include the power source, the spectrum analyser, power source, microcontroller and the connecting wires.

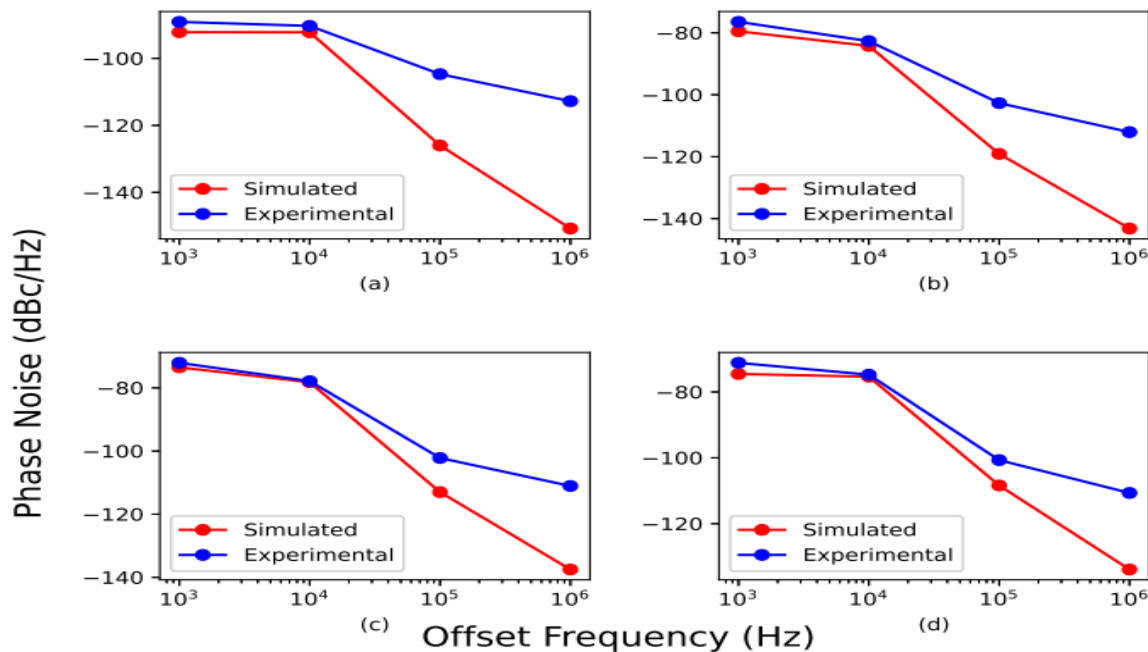


Figure 13: A comparison of the phase noise of simulated and experimental data at (a) 387 MHz, (b) 1 GHz, (c) 2 GHz and (d) 2.9 GHz

Experimental Spurs

Most of the spurs observed at 387.00 MHz output frequency were harmonics as shown in Figure 14. At full span, we were able to observe up to the fifth harmonic. The level of the first, second, third, fourth and fifth harmonics were -33.1 dBm, -75.7 dBm, -51.7 dBm, -77.6 dBm, -66.3 dBm and -77.2 dBm respectively as shown in Table 5.

Table 5: Level of spurs at 387.00 MHz output frequency

Frequency (MHz)	Level (dBm)	Level (dBc)
50	-73.3	-40.2
100	-75	-41.9
387	-33.1	0
600	-71.6	-38.5
774	-75.7	-42.6
940	-76.4	-43.3
1161	-51.7	-18.6
1548	-77.6	-44.5
1935	-66.3	-33.2
2320	-77.2	-44.1
2700	-70.5	-37.4

There were other spurs observed at 387.00 MHz output frequency as shown in Figure 14. These spurs appeared at 50 MHz, 100 MHz, 600 MHz, 940 MHz, 2320 MHz and 2700 MHz frequencies and after calculation, their level with respect to the carrier was found to be -40.2 dBc, -41.9 dBc, -38.5 dBc, -43.3 dBc, -44.1 dBc and -37.4 dBc respectively as shown in Table 5. These spurs could be contributed by the reference frequency oscillator because they appeared at multiples of input reference frequency of 10 MHz. Another possible cause could be the channel spacing used while designing the PLL of 100 kHz. This is because these spurs also appeared at multiples of the channel spacing.

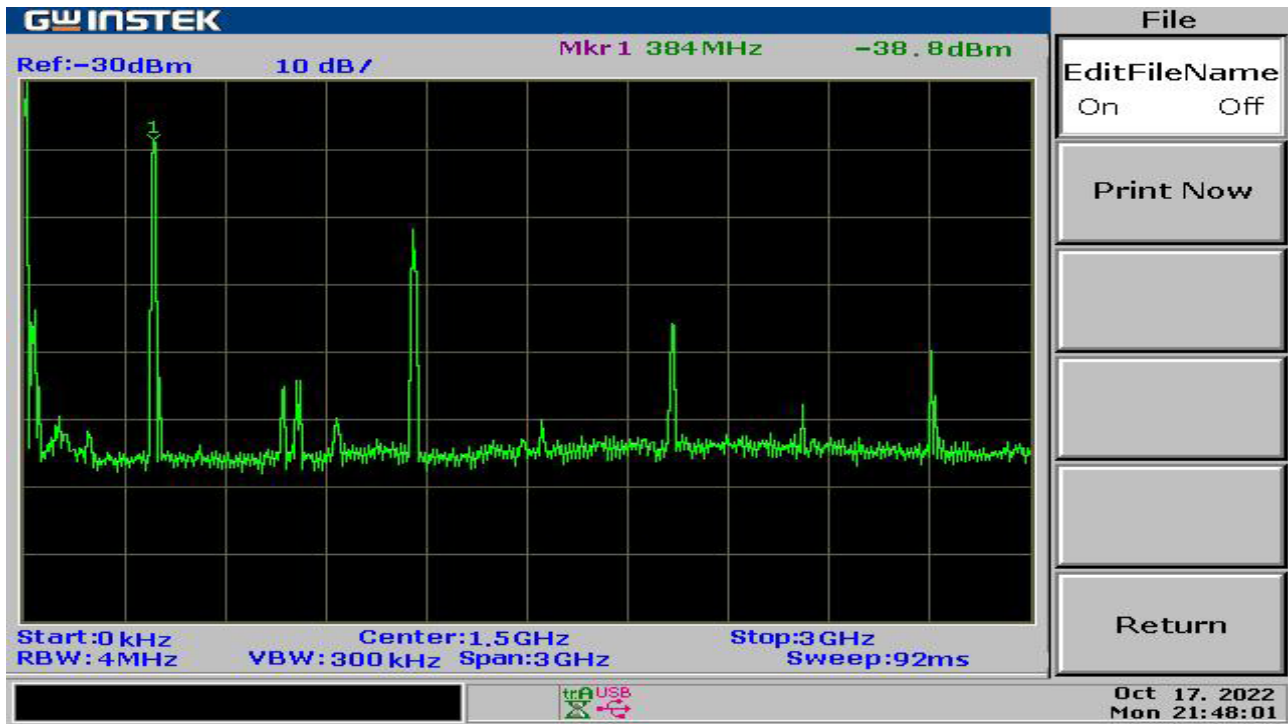


Figure 14: Level of spurs at 387.00 MHz output frequency

CONCLUSION

The simulation and design of a Phase-Locked-Loop based signal generator which can generate frequencies in the range of 35 MHz-3 GHz, with a 1 kHz frequency step and with a low level of phase noise using a PLL based synthesizer is reported. The simulation is done using ADIsimPLL design software and the Phase-Locked-Loop chip used is the ADF4351 from Analog Devices. The PLL is simulated at different values of loop bandwidth and an optimum value of 10 kHz is obtained. The simulations are also done for different values of phase margin and an optimum value of 45° is obtained by analyzing the resultant phase noise and lock time. The noise of each PLL component is analysed and their effects are presented in this paper. The signal generator had a phase noise of -102.6 dBc/Hz and -102.2 dBc/Hz at a 100 kHz offset frequency for 1 GHz and 2 GHz output frequencies, respectively. The experimental phase noise was higher than simulated phase noise, and the phase noise also increased with an increase in output frequency. The maximum spur appeared at the third harmonic and was found to be -18.6 dBc, while the minimum spur appeared at the fourth harmonic and was found to be -44.5 dBc. This design has improved the phase noise performance for the signal generator with a wide range of output frequencies.

RECOMMENDATIONS

The signal generator developed in this study has practical applications in the electronics lab for testing RF components like Wifi, GPS, and wireless communication

systems. It proves valuable during the design and debugging process. Additionally, this signal generator can effectively characterize microstrip antennas within the lab setting. Furthermore, the proposed signal generator can be easily adjusted to allow users to select their desired peak-to-peak voltage for the output frequency, based on the specific requirements of their application. This flexibility enhances its usability and adaptability.

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