Multipliers Design using Machine Learning Algorithms for Energy Efficiency

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†ABSTRACT

Designers primary goal is to develop the Adder cell with improved performance viz. speed, fixed rise and fall time, as it the fundamental block in VLSI design process. The dynamic logic circuits are far better than the static logic circuits because it consumes less power and speed performance also increased. But, cascading of several blocks in dynamic logic is found to be a wrong analysis. This drawback of increased complexity with mismatched cascading is overcome by using domino logic circuits. By using domino logic circuits, the reduction of noise margins and increase the speed performance of the circuit is achieved. In this paper, domino logic based Manchester carry chain adder (MCC) is designed using FinFET 18nm technology in Cadence virtuoso. It is noticed that 4-bit and an 8-bit Manchester Carry Chain Adder (MCC) using domino logic design consumes less power and reduction in the delay of the proposed circuit compared with the previous architecture. Implementation results reveal that the 4-Bit MCC Adder has delay of 79.45% less compared to the existed standard design and power consumption also reduced to 94.15%.

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INTRODUCTION

MCC Adder mainly work on propagate and generate signals. MCC uses carry generate and carry propagate signal to determine the carry for every stage. This carry generate and carry propagate signals are calculated in advance. MCC requires a redundant stage to give input carry and also an input clock signal. In ripple-carry adder (RCA) architectures, the generated carry in first stage is passed to the next stage and up to N-stages. The overall path delay of RCA is expressed mathematically as follows:

\[ t_{delay} = t_{sum} + (N-1)t_{carry} \]

Where \( t_{carry} \) and \( t_{sum} \) are related to the propagation delays of sum and carry output from first stage to N-stages where N is the total number of stages of the adder module design. From the above equation (1), the majority of total delay of an adder circuit is contributed by \( t_{carry} \). Thus, there is a need to reduce the delay belong to the carry generation path. MCC optimizes the propagation delay related to carry path \( t_{carry} \). Therefore, this carry chain improve the speed performance of the addition process of the overall adder block involved. The functional verification of the adder blocks is validated with the following Table 1.

<table>
<thead>
<tr>
<th>Cin</th>
<th>B</th>
<th>A</th>
<th>Sum</th>
<th>Cout</th>
<th>Carry status</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Generate</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Generate</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Propagate</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Propagate</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Propagate</td>
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<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Propagate</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Delete</td>
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<td>0</td>
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<td>0</td>
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<td>Delete</td>
</tr>
</tbody>
</table>
The existing system of MCC adder is designed using CMOS at 180nm technology. The entire circuit design and simulation were done using cadence Tool. The existing MCC adder was designed using dynamic logic circuits. When the dynamic logic MCC adder is compared with the conventional logic circuit, the delay of the circuits is reduced but the power consumption was increased. The major drawback of the existing circuits is power consumption. The channel length is also large.[28-31]

The proposed system of 8-bit MCC adder is designed using FinFET at 18nm technology. The entire circuit design and simulation were done using cadence tool. The proposed circuit has many advantages like suppressed short channel effect, very less channel length, the delay of the circuit is optimized and power consumption is also reduced compared with the previous design.[32-39]

This paper is organized as follows; Section II describes the literature survey on FinFET transistors structural features followed by section III, which discuss about the proposed MCC Adder models. Section IV presents the cadence-based simulation results and their analysis. Section V elaborates the experimental findings of FinFET based MCC Adder. Section VI gives the conclusion of the paper including features and limitations followed by references.

**Fundamental Design Aspects of FinFET**

FinFET is the structural representation for fin shaped field effect transistor. Chenming Hu with support from his teammates has successfully modeled FinFET. The main objective behind the structure is having a thin body, then the gate capacitance is near to the channel .10nm or less than that width thin is the body. These leads to leakage path far away from the gate can effectively control the leakage.[32-35]

Bulk silicon or silicon on insulator (SOI) wafers are used for implementation of FinFET. The substrate consists of a thin fin of silicon body. The three sides of the channel are controlled due to wrapping of gate around the channel. The structure is said to be FinFET since Si body similar to the fish’s back fin. The below Fig. 1 represents the 3-D model of FinFET structure.[16]

Bulk MOS has the channel which is horizontal. Where as in FinFET the Channel is vertical. Width of device is Height of the channel (Fin) in the FinFET. Perfect Width of Channel is given by

\[
\text{Width of channel} = 2 \times \text{Fin Height} + \text{Fin width} (2)
\]

Increase in the height of the channel fin leads to increase in the width therefore leads to increase in the drive current of FinFET. Parallel construction of multiple fins connected together shown in Fig. 3 also leads to increase in the device drive current. Devices drive strength can be determined by varying channel width seen in Planar devices.[17-19]

Reduction in short channel effects and ensuring high \(V_T\) (Threshold) is seen in conventional MOS, where as in FinFET provides better SCE (Short Channel Effect), therefore doping of channel become optional this is due to wrapping of gate structure around the channel and body is thin. The fundamental variation of the MOSFET and FinFET is summarized in the Table 2.

**Proposed Adder Models**

**8-Bit MCC Adder**

The 8-bit MCC Adder is applicable to optimize the delay and to increase the speed of the circuit. The 8-bit MCC Adder is mainly used instead of 4-bit MCC Adder as a building block, can lead to most efficient and high-speed adder implementation. The 8-bit MCC Adder consists of two 8-bit inputs namely \(P\),
Table 2: Comparison Table of FinFET and MOSFET

<table>
<thead>
<tr>
<th>MOSFET</th>
<th>FinFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lower driven currents</td>
<td>Higher driven currents</td>
</tr>
<tr>
<td>High leakage currents</td>
<td>Low leakage currents</td>
</tr>
<tr>
<td>Short Channel Effect is present</td>
<td>Suppressed Short Channel Effect (SCE)</td>
</tr>
<tr>
<td>It consumes more power</td>
<td>It consumes less power</td>
</tr>
<tr>
<td>Scaling and Mobility of transistor is not applicable for less than 40nm</td>
<td>Scaling and Mobility of transistor is applicable less than 28nm</td>
</tr>
</tbody>
</table>

Fig. 4: 8-bit MCC Adder

The 8-bit MCC Adder is designed using FinFET technology to reduce power consumption and improve efficiency. The inputs to the MCC are the 8-bit operands A and B, and the outputs are the sum S and carry C. The 8-bit MCC Adder consists of 8 stages, each performing a carry generate (G) and carry propagate (P) operation.

P, G, and C operate as follows:

Case 1: When A=0 and B=0
If Clk=1, P=A, G=A, C=A
In this case, the output is 0, and the carry is 0.

Case 2: When A=1 and B=0
If Clk=1, P=A, G=A, C=1
In this case, the output is 1, and the carry is 1.

Case 3: When A=1 and B=1
If Clk=1, P=A, G=A, C=0
In this case, the output is 2, and the carry is 0.

Case 4: When A=0 and B=1
If Clk=1, P=A, G=A, C=0
In this case, the output is 1, and the carry is 0.

Fig. 5: 4-bit MCC Adder

The 4-bit MCC Adder is a simpler version of the 8-bit MCC Adder, designed to handle 4-bit inputs. It consists of 4 stages, each performing a carry generate (G) and carry propagate (P) operation. The inputs are A and B, and the outputs are the sum S and carry C. The 4-bit MCC Adder is useful in applications where 4-bit data processing is sufficient.

Outcomes of the Standard Models

4-bit MCC Adder

The 4-bit MCC Adder is designed using FinFET technology to reduce power consumption and improve efficiency. The inputs to the MCC are the 4-bit operands A and B, and the outputs are the sum S and carry C. The 4-bit MCC Adder consists of 4 stages, each performing a carry generate (G) and carry propagate (P) operation. The inputs to the MCC are the 4-bit operands A and B, and the outputs are the sum S and carry C. The 4-bit MCC Adder is useful in applications where 4-bit data processing is sufficient.
too has designed using the same FinFET models. Similarly, the propagation and generation signal symbol are created which has multiple number of n-LVT and p-LVT.

**Transient response of 4-Bit MCC adder**

The response of a system to a change from a steady state or equilibrium state is known as Transient response. The transient is not definitely tied to on or off state, but to any state that affects the steady state of the system.

The schematic diagrams or circuit design of 4-bit and 8-bit MCC Adder are simulated using Cadence software and FinFET 18nm technology to obtain transient response.

From the transient response figures, 0V represents logic ‘0’ which implies ‘OFF’ state and where as 1V represents logic ‘1’ which implies ‘ON’ state.

In FinFET, the maximum voltage is considered up to 1V. This means that $V_{DD}$ is 1V and GND is 0V. FinFET cannot withstand high voltages that are greater than 1V as it leads to the damage of transistors.

The Fig. 7 represents the transient response of 4-bit MCC Adder. The entire simulation is done using Cadence virtuoso at FinFET 18nm technology.

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**Experimental Findings**

Using Cadence virtuoso FinFET 18nm spectre models, the following outcomes for 4-bit MCC Adders are observed.

**Delay Metric**

It is observed from the above delay analysis Table 3, the propagation delay of the proposed design has the considerable impact of delay reduction. The proposed design has reduced delay value of 0.1013ns. When compared with previous design of 4-bit MCC Adder, the proposed model has reduced delay of about 80% less.

**Power Metric**

From the Table 4, the power consumption of the proposed circuit is also reduced. The proposed design has reduced power consumption value of 1.005uW. When compared with previous standard design, the energy dissipation for the design of the circuit shown in Fig. 6 is reduced by 94.15%.

The PDP values presented in the above Table V shows the reduction of the PDP metric compare to that of previous standard models. PDP for the design of Fig. 6 is reduced by 98.79% to the original conventional MOS transistor version.

It can be noticed from the above EDP analysis Table VI, hence from previous delay and PDP measures too, even EDP also has the proportionate minimized value. When compared with previous standard design, the EDP for the design of Fig. 6 is reduced by 99.75%.

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<table>
<thead>
<tr>
<th>Existing design (4-Bit MCC Adder)</th>
<th>Proposed design (4-Bit MCC Adder)</th>
<th>Change in delay (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.493ns</td>
<td>0.1013ns</td>
<td>79.45% Decrease</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Existing design (4-Bit MCC Adder)</th>
<th>Proposed design (4-Bit MCC Adder)</th>
<th>Change in delay (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>17.18uW</td>
<td>1.005uW</td>
<td>94.15% Decrease</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Existing design (4-Bit MCC Adder)</th>
<th>Proposed design (4-Bit MCC Adder)</th>
<th>Change in PDP (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>8.47*10^-15J</td>
<td>1.02*10^-16J</td>
<td>98.79% Decrease</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Existing design (4-Bit MCC Adder)</th>
<th>Proposed design (4-Bit MCC Adder)</th>
<th>Change in EDP (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.175*10^-24Js</td>
<td>1.033*10^-26Js</td>
<td>99.75% Decrease</td>
</tr>
</tbody>
</table>
CONCLUSION

Cadence virtuoso is used to design and simulate the MCC circuits. There is an excellent improvement in reduction of the power consumption and delay of the proposed circuit and the performance and speed of the circuit is increased. The performance is analysed by using 18nm FinFET spectre models. The simulation results demonstrates reduced power consumption and delay values of 4-bit and 8-bit MCC Adders. The reduced power and delay values of 4-bit MCC Adder are 1.005uW and 0.1013ns, respectively. When compared with previous design of 4-bit MCC Adder, the delay of the proposed FinFET based circuit reduced by 79.45%. It also observed that the power consumption of 4-bit MCC Adder compared with previous design is reduced by 94.15%. Hence, the proposed 4-bit and 8-bit MCC Adders are highly efficient compared with the previous design. As a further work minimization of the distortions through various combinations of logics and designing the MCC adders for complex circuits or higher variables like 16, 32, 64 bit can be done. The paper further extended by reducing the channel length or designing in submicron technology and decreasing the area of this chain.

REFERENCES


[27] Dr. L.V. Narasimha Prasad, Dr. Vijay Vallabhuni, Dr. S. China Venkateswarlu, Dr. V. Vhandra Jagan Mohan, Ms. P. Sruthihaya, Mr. K. Tarun Kumar, Mr. B. Raju, Mr. P. Ravinder, “Garbage Collector with Smart Segregation and Method of Segregation Thereof,” The Patent Office Journal No. 04/2022, India. Application No. 202141062770 A.


[36] Chandra Shaker Pittalla, Vallabhuni Vijay, B. Naresh Kumar Reddy, “1-Bit FinFET Carry Cells for Low Voltage High-
